

Method for Reducing Defects in Post Passivation Interconnect Process

ABSTRACT

A method of forming post passivation interconnects for an integrated circuit is disclosed. A passivation layer of a non-oxide material is formed over the integrated circuit. A buffer layer is then formed over the passivation layer. The buffer layer preferably is a silicon oxide layer with a thickness substantially smaller than a thickness of the passivation layer. A post passivation metal layer is deposited over the buffer layer and a connection pattern is formed in the post passivation metal layer.